Agilent Technologies

Debug Your Embedded Design More Quickly

August 19th, 2003

presented by:

Mike Beyers
Oscilloscopes Project Manager

Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- “Late in the Game” Debug Process Recommendations
- Recommended Agilent Products
- Additional References

Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- “Late in the Game” Debug Process Recommendations
- Recommended Agilent Products
- Additional References

Agilent Technologies

Trends in Embedded Systems - Past

- 20 Years ago each embedded processor system was a unique design.
- The processor had no internal memory or IO control.
- Therefore memory and IO control was kept relatively simple.
- Digital signals were easily probed with a four channel analog oscilloscope.

Agilent Technologies

Trends in Embedded Systems - Today

- Today, processors and FPGAs can include complex memory and IO control systems.
- Technologies like SDRAM for memory and PCI for IO have migrated from high-end computers to mid-range embedded systems in only a handful of years.
- The modern embedded system designer will need a variety of tools when debugging these more complex systems.

Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- “Late in the Game” Debug Process Recommendations
- Recommended Agilent Products
- Additional References

Agilent Technologies

SDRAM Control Signals.

- **Need to view 5 digital signals to identify/trigger on a particular cycle - the three to the right plus chip select and Clock.**
- **Need to look *at least* clock and another line (address, data or control) with analog channels to verify timing and signal integrity.**
- **Operation is pipelined.**

SDRAM Commands

Command	RASN	CASN	WEN
No Operation (NOP)	H	H	H
Active (ACT)	L	H	H
Read (RD)	H	L	H
Write (WR)	H	L	L
Burst Terminate (BT)	H	H	L
Precharge (PCH)	L	H	L
Autorefresh (ARF)	L	L	H
Load Mode Register (LMR)	L	L	L

Agilent Technologies

PCI Control Signals.

- **PCI is a very complex protocol. *The PCI bus specification is 322 pages!* But it is commonly used and cheap to implement..**
- **Besides the 4 command lines, there are 6 control lines (FRAME#, TRDY#, IRDY#, STOP#, DEVSEL# and IDSEL), 2 error signals, 2 arbitration signals, and a clock and reset line.**

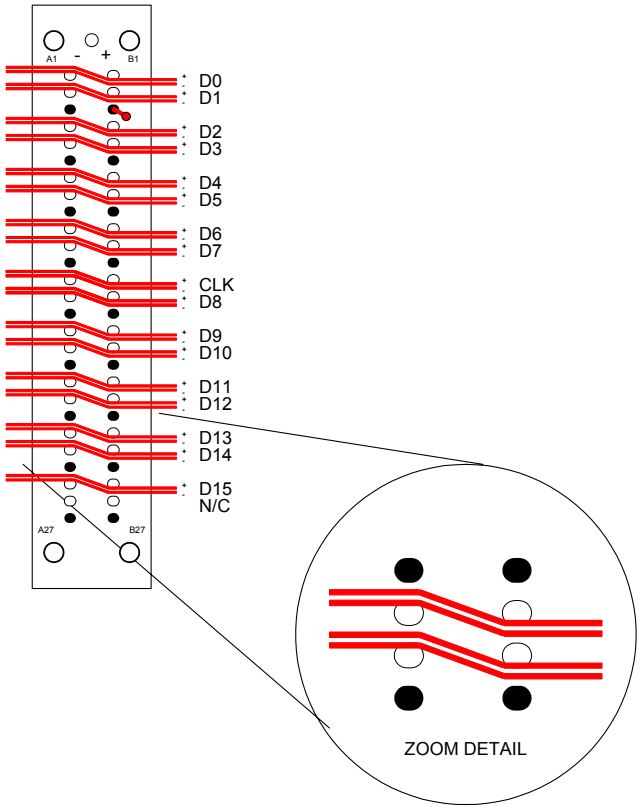
PCI Commands

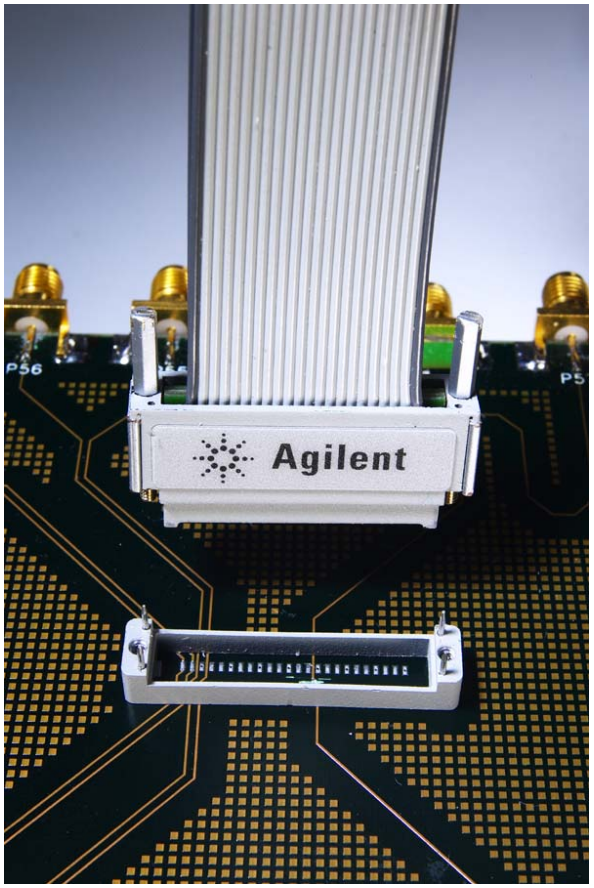
C/BE[3:0]#	Command Types
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

Agilent Technologies

Hint #1: Add LA Connector Footprints

- The user puts down a ‘landing pattern’ on the target system.
- The connector-less probe is then attached to the system with a ‘retention module’





Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- “Late in the Game” Debug Process Recommendations
- Recommended Agilent Products
- Additional References

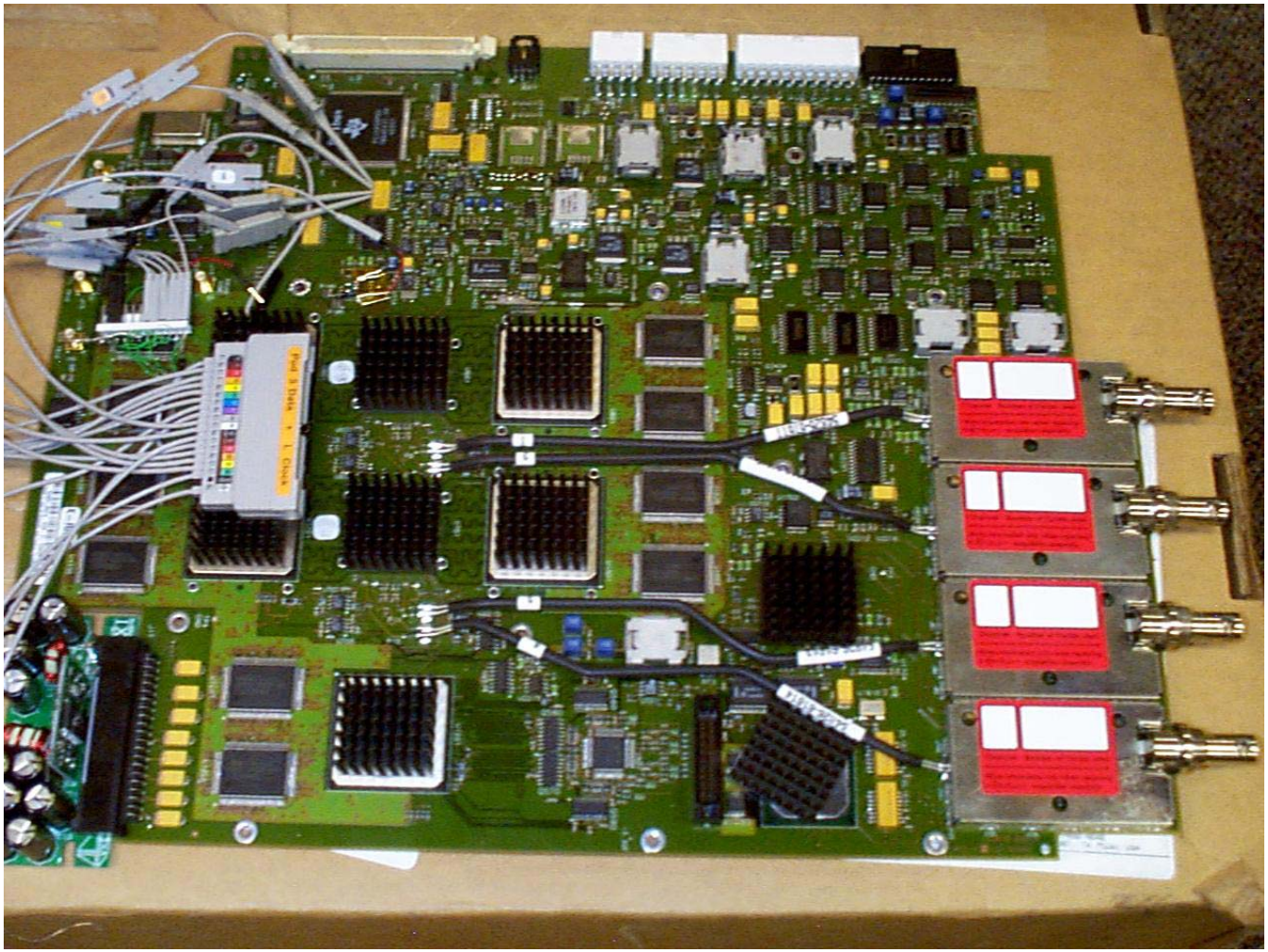
Agilent Technologies

Hint #2, 3, 4: Start with Raw Board

- **Hint #2:** Check for ground and power plane shorts with DMM. Check loaded board too!
- **Hint #3:** Check R across power planes and calculate expected IR loss.
- **Hint #4:** Check controlled impedance lines with TDR. Concentrate on Clock traces, as they are most sensitive in syncronous systems like SDRAM and PCI.

Agilent Technologies

Loaded Board Turn-On



Agilent Technologies

Hint #5: Check Supplies with Scope

- Use Scope instead of DMM - see noise and dynamic loading issues. Modern CMOS devices can load down a PS when they come out of reset or do a burst of memory or IO accesses.
- Re-check supplies once everything is working. Power consumption is dependant on operation.
- Check with current probe if supply droops.

Hint #6: Check PS Sequencing

- Modern IC's often use several different supply voltages - for core and IO.
- Follow manufacturer's recommendation (On and Off!).
- Consider distributed power with DC-DC conversion off one rail. Soft start options allow control of power supply sequencing.
- Rule of thumb - bring all supplies up together if no manufacturer's recommendation.

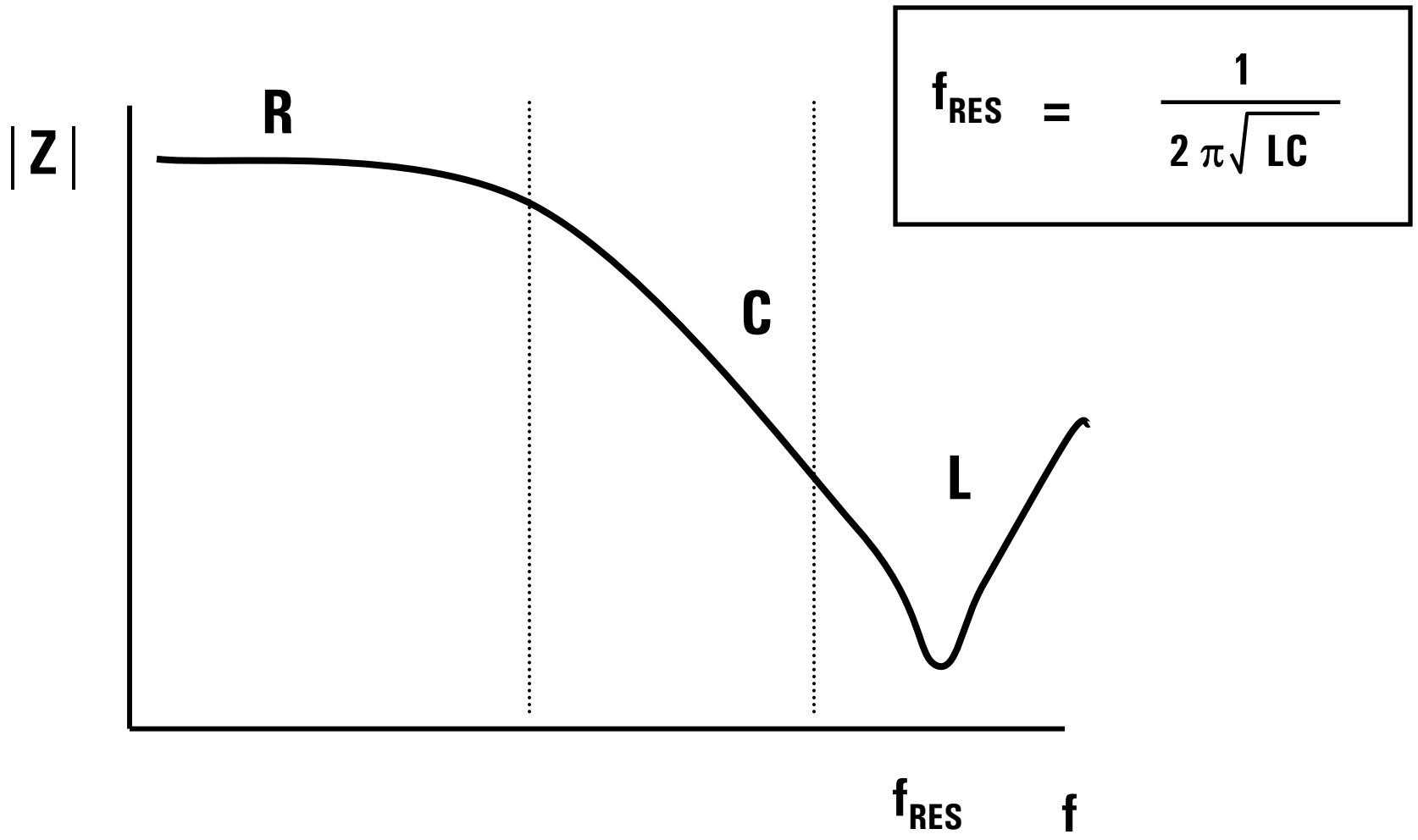
Agilent Technologies

Next Step - Look for Clocks.

- Clocks will normally be your highest speed signals.
- Edge rates are probably 1ns or less.
- BW_{Signal} ~= 0.5 / risetime.
- Hint #7: $BW_{Measurement}$ needed = 1 / risetime for ~5% error. (1ns risetime = 1GHz). Remember, $BW_{Measurement}$ is often limited by $BW_{Accessories}$!

Agilent Technologies

Consider Probe Loading



Agilent Technologies

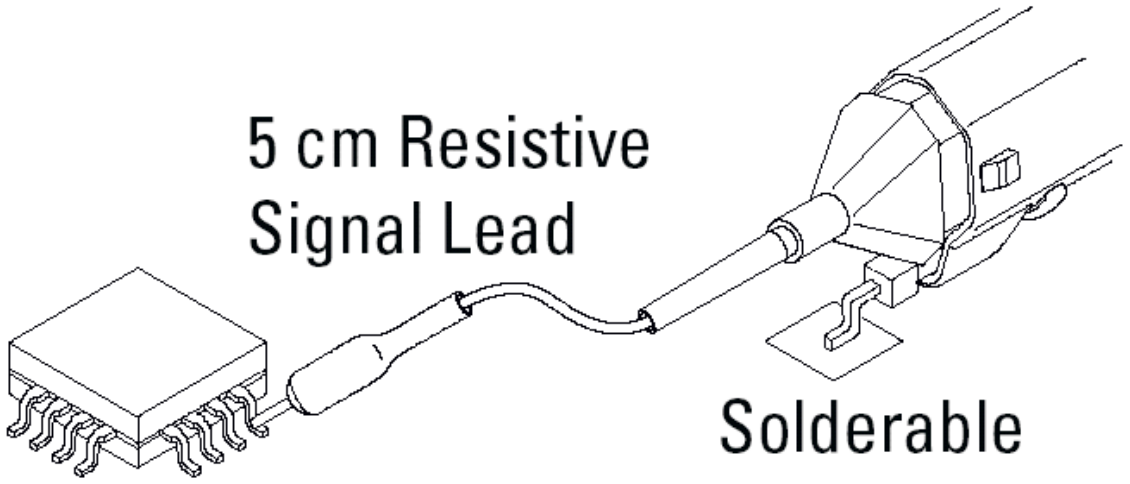
Hint #8: Use 1nH/mm to Estimate f_{RES}

1156A Active Probe
w/5cm signal lead
Input C = 0.8pF
L = 50nH
f_{RES} = ~850MHz

1165A Passive Probe
w/10cm ground lead
Input C = 9pF
L = 100nH
f_{RES} = ~167MHz

Agilent Technologies

1156A Recommended Configurations



This configuration works with either 2s or 3s as signal and either 2g or 3g as ground.

BW ≅ 1.4 GHz

Agilent Technologies

Hint #9: Check Loading with 2 Probes

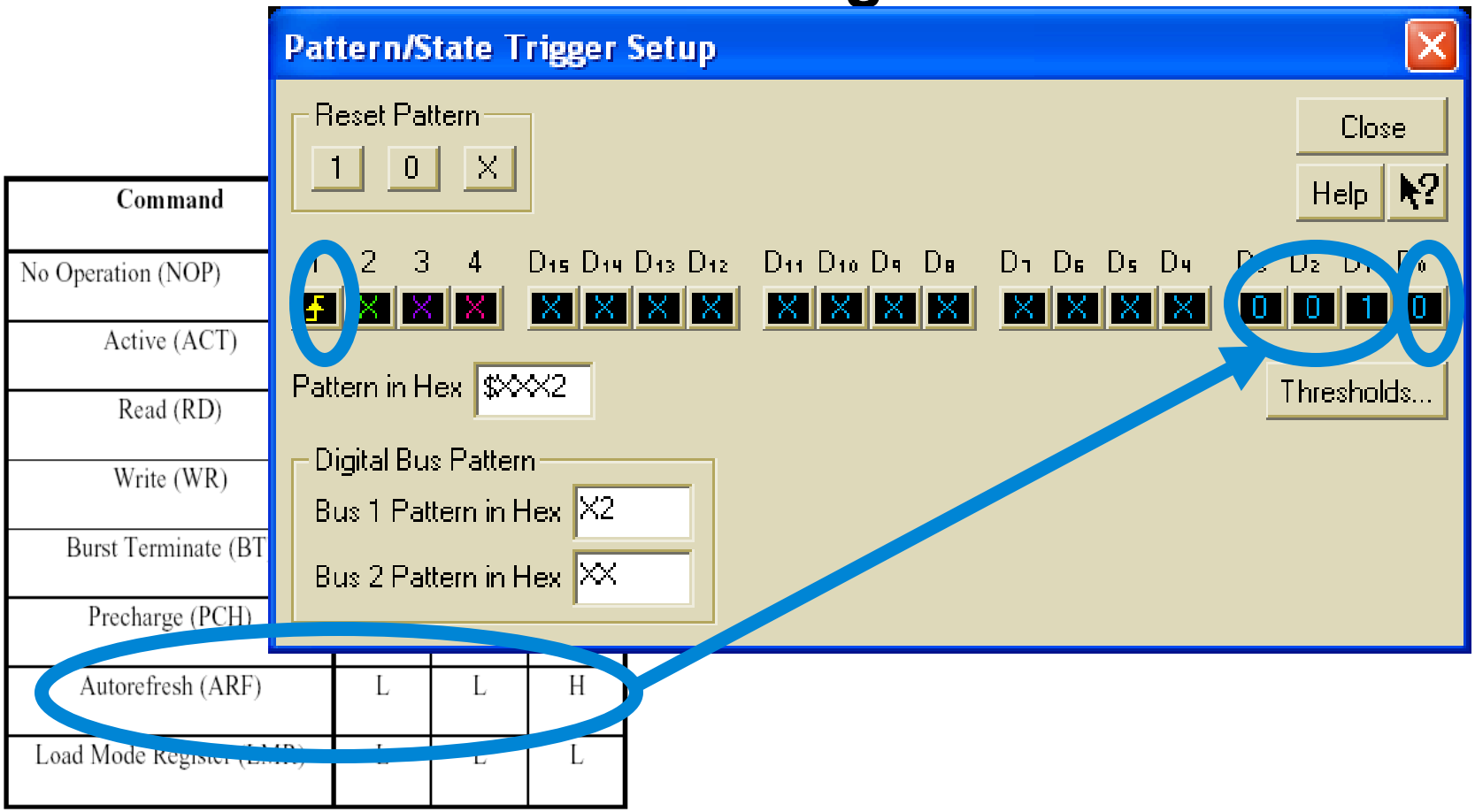
Agilent Technologies

Clock Hints

- **Hint #10:** Always probe clocks at receiver.
- **Hint #11:** Probe LVDS clocks differentially (Zero crossing most important).
- **Hint #12:** Trigger on slowest clock when looking at divided clocks.
- **Hint #13:** Clock Layout: Avoid vias, split ground and power planes, and sharp corners. Layout power first, clocks next, then everything else.
- **Hint #14:** Recheck clocks after everything is turned on. May uncover data dependant coupling!

Next Challenge - The Memory System

- **Hint #15: Start off checking for Refresh.**



Agilent Technologies

Hint #16: Isolate a Single Cycle

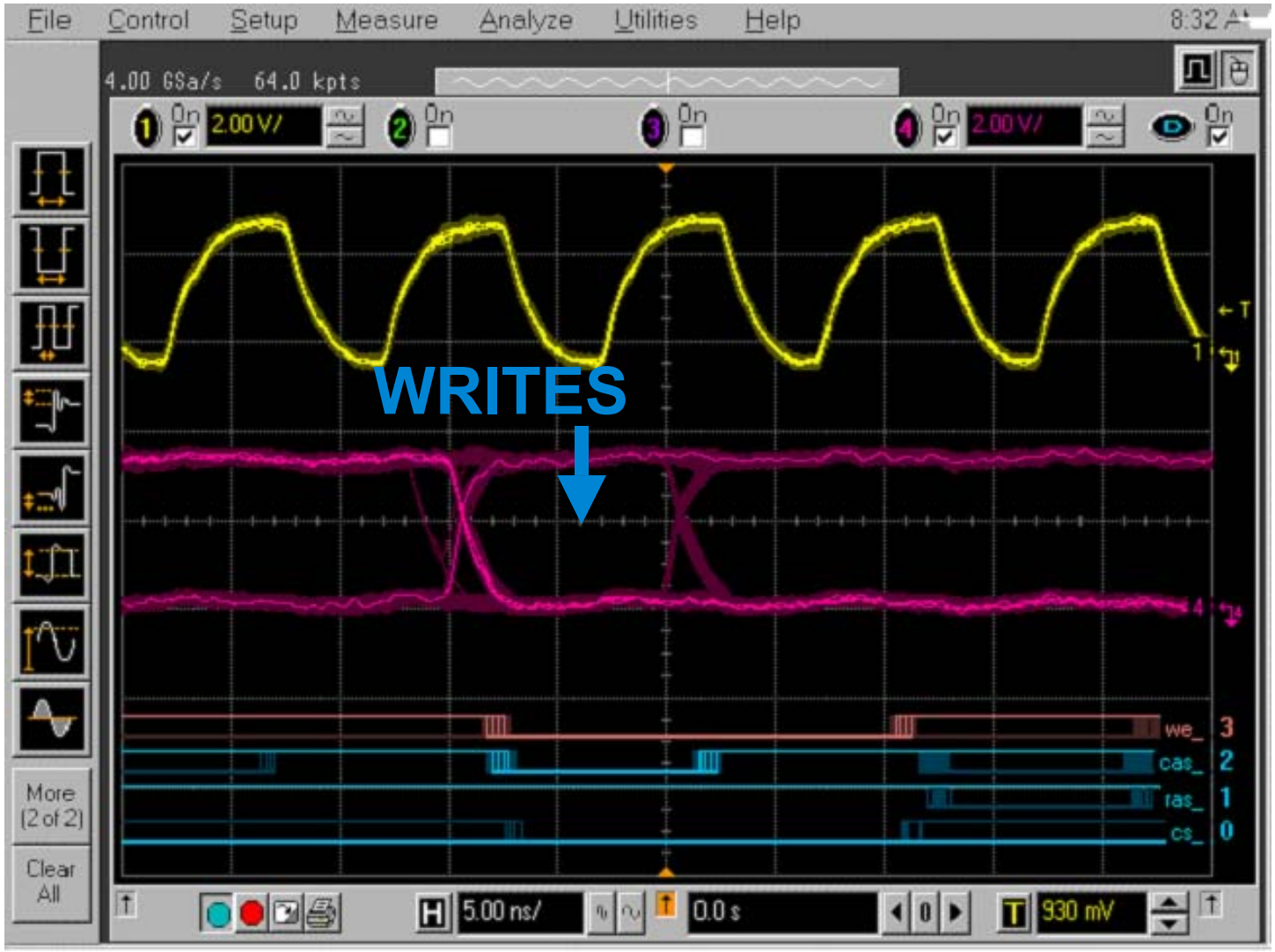
- Use special firmware or HDL to generate a continuous stream of just writes, then just reads.
- Vary data: All 1's, all 0's, checkerboards, to get more transistions.
- Look for illegal logic levels, setup/hold violations. Check direction control on buffers.
- Check many address and data lines. Note worst ones (timing and signal integrity) for future work.

Hint #17: Probe the Right End

- Probe address and data writes at memory.
- Probe data reads at controller.
- Probe clocks at memory.

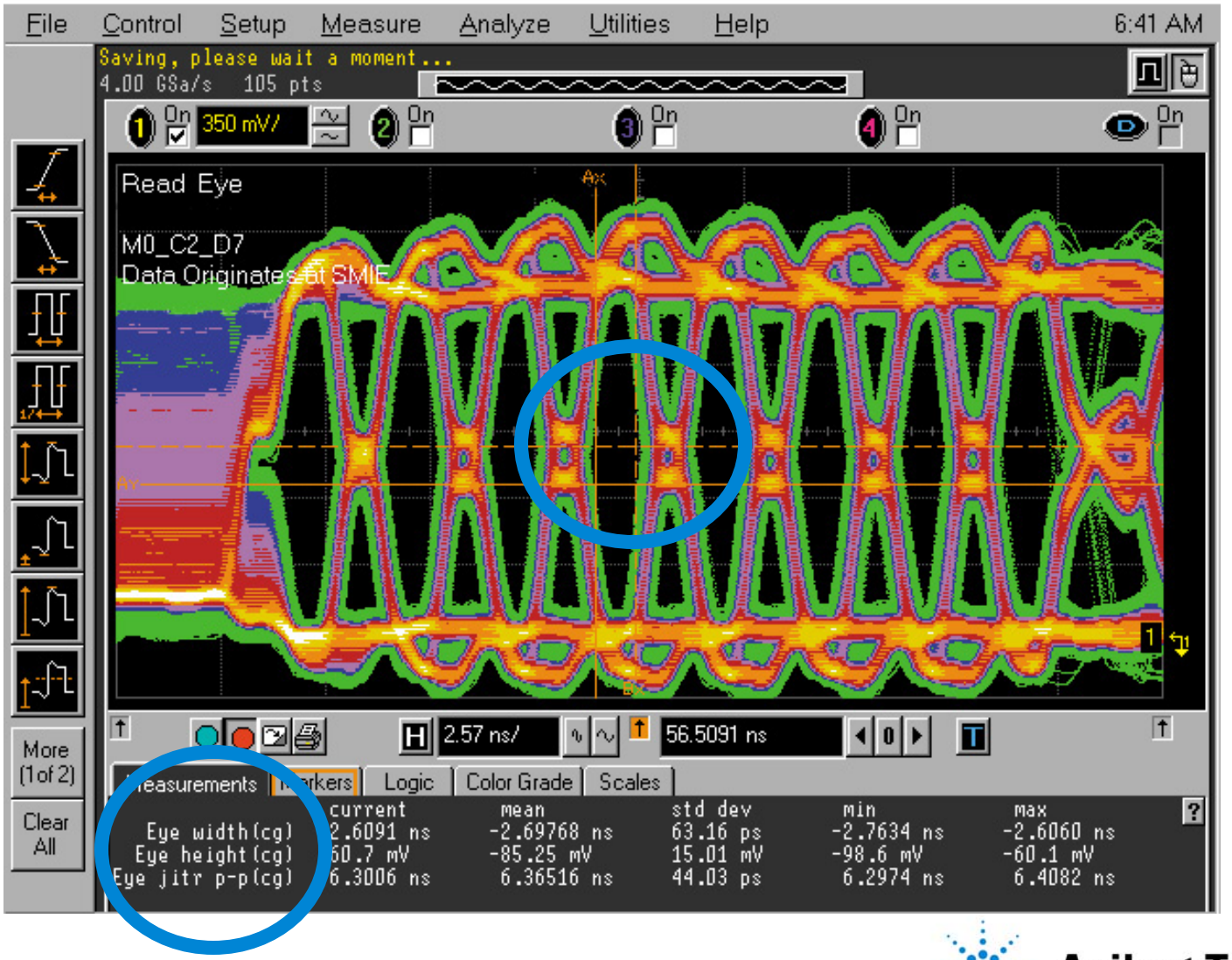
Agilent Technologies

Hint #18: Pattern Trigger Isolates Cycles



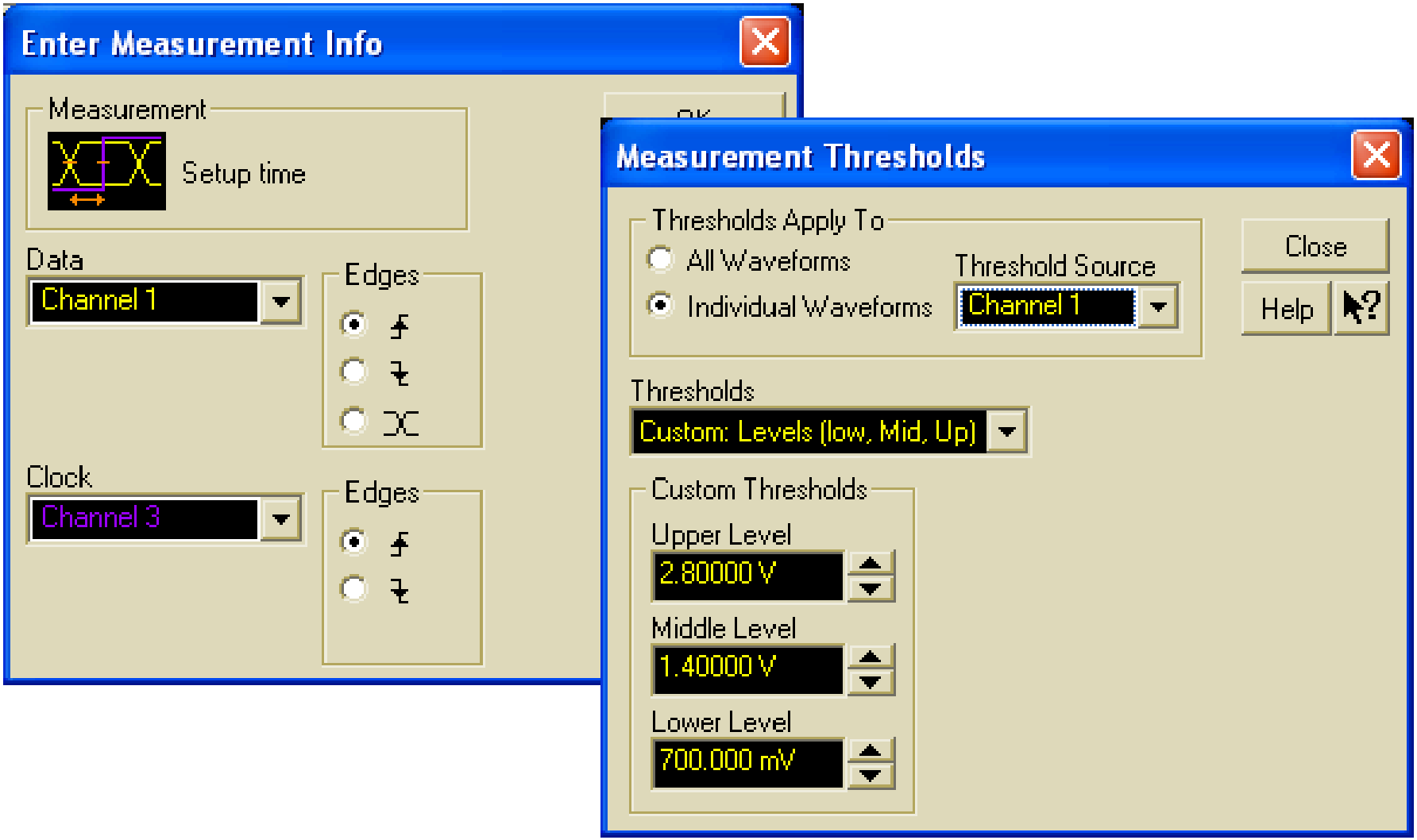
Agilent Technologies

DDR SDRAM Burst Read Example



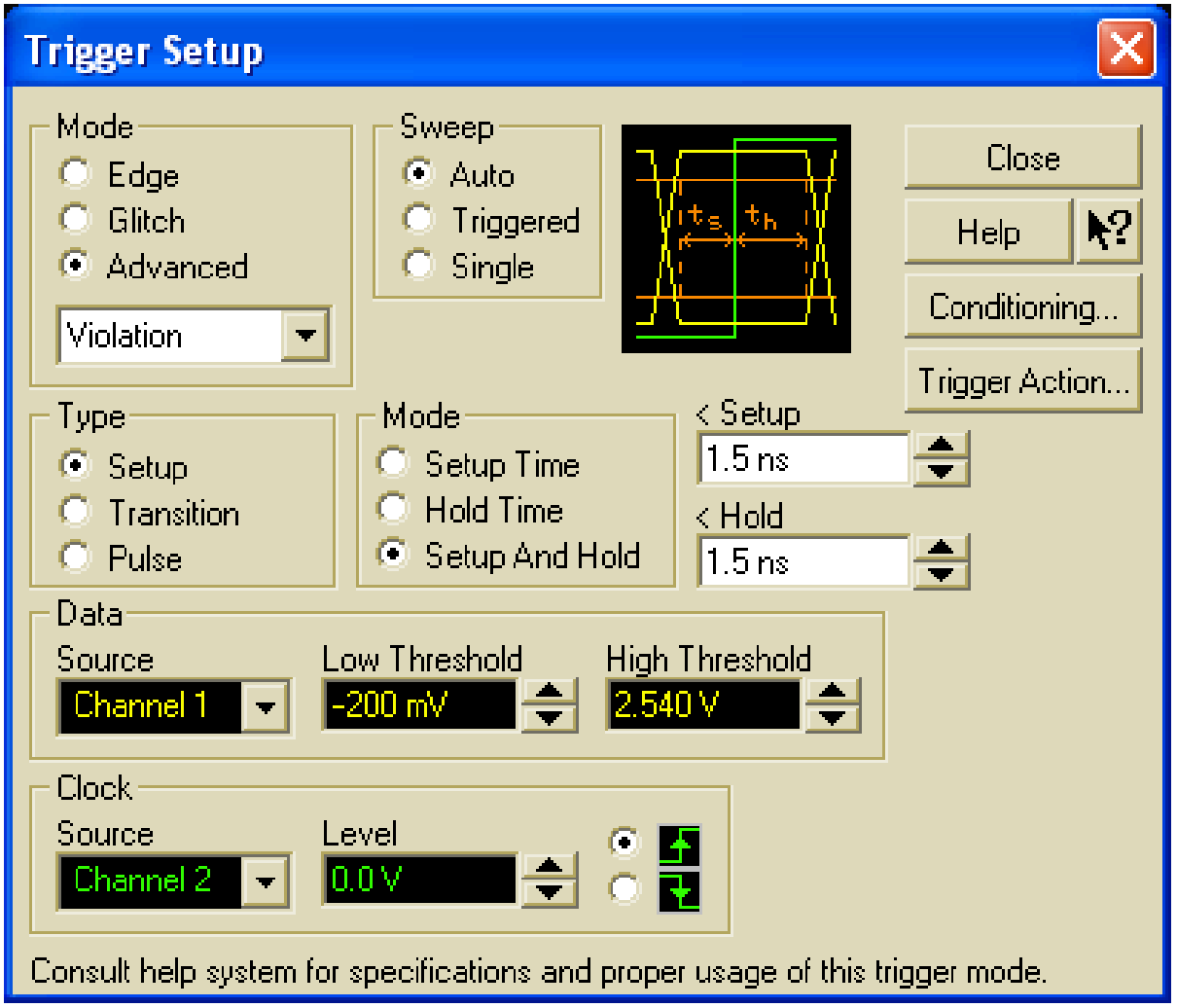
Agilent Technologies

Hint #19: Use Custom Thresholds



Agilent Technologies

Hint #20: Use Violation Triggering



Agilent Technologies

Hint #21: Read the Fine Print

- Some vendors specify minimum risetime.
- Some specifications are functions of risetime.
- Some vendors specify N refreshes before use.
- Look for clock output R. Series terminate clocks with $R_{term} = R_{line} - R_{source.}$
- Vary temperature if margin is small. Specs are tighter than they used to be!
- Verify revision of specification = revision of silicon.

Agilent Technologies

Hint #22: Recheck Clocks and Refresh

- After system is up and running - recheck clock signal integrity and worse case setup/hold lines. Look for data dependant problems.
- Also check refresh cycles. Sometimes controllers refresh fine with little memory activity but can leave out refresh as memory traffic increases.

PCI Bus turn on hints

- **Again, clocks are most critical. Clocks are point to point - series terminated.**
- **Hint #23: Give clock traces more space even if you have to squeeze AD and control.**
- **Hint #24: Length dictates speed (33MHz or 66MHz) and minimizes timing margin. Do not approach length limits unless absolutely necessary.**

Pause for Q&A

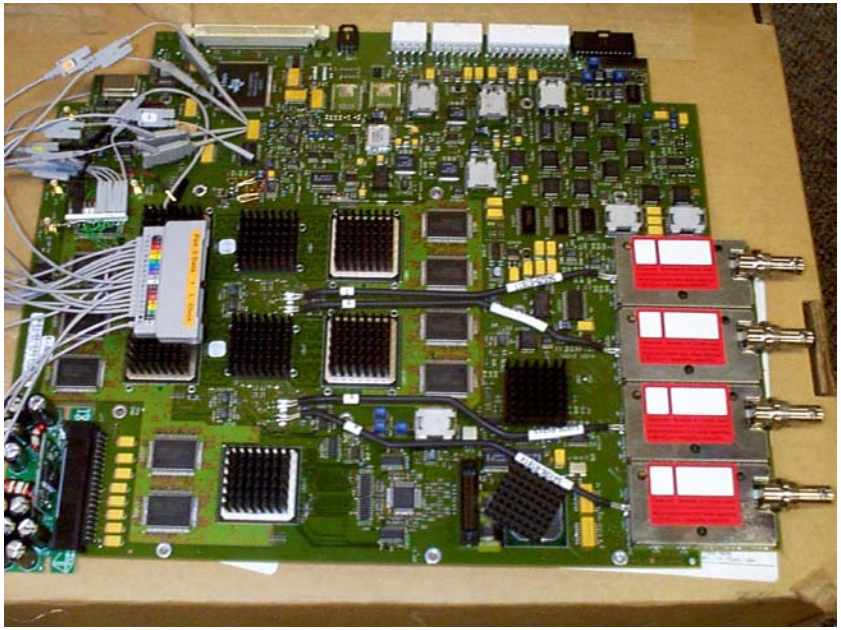
Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- "Late in the Game" Debug Process Recommendations
- Recommended Agilent Products
- Additional References

Agilent Technologies

Example: PCI Bus Intermittent Lockup



Acquisition Board of 54832D

- Has 125MHz SDRAM for memory and 33MHz PCI bus for communication between ASICs and Host PC.
- SDRAM worked fine. PCI bus had problems that threatened to delay shipments.
- Team did not plan ahead - no logic analyzer connectors for PCI bus on acquisition board.

Agilent Technologies

Situation & Challenges

- The problem happened very occasionally, and only on a few units.
- They had no idea where the write was going astray.
- They could easily hook up to Bus 1 (Backplane) and with some effort hook up to Bus 2 (Ribbon Cable), but found it nearly impossible to hook up to Bus 3 (SMT to BGA routing).

Hint #23: Break It Before You Fix It

- Look for units that fail most often.
- Modify firmware/HDL to fail more often.
- Vary temperature to fail more often.
- Duplicate failure in simulation.

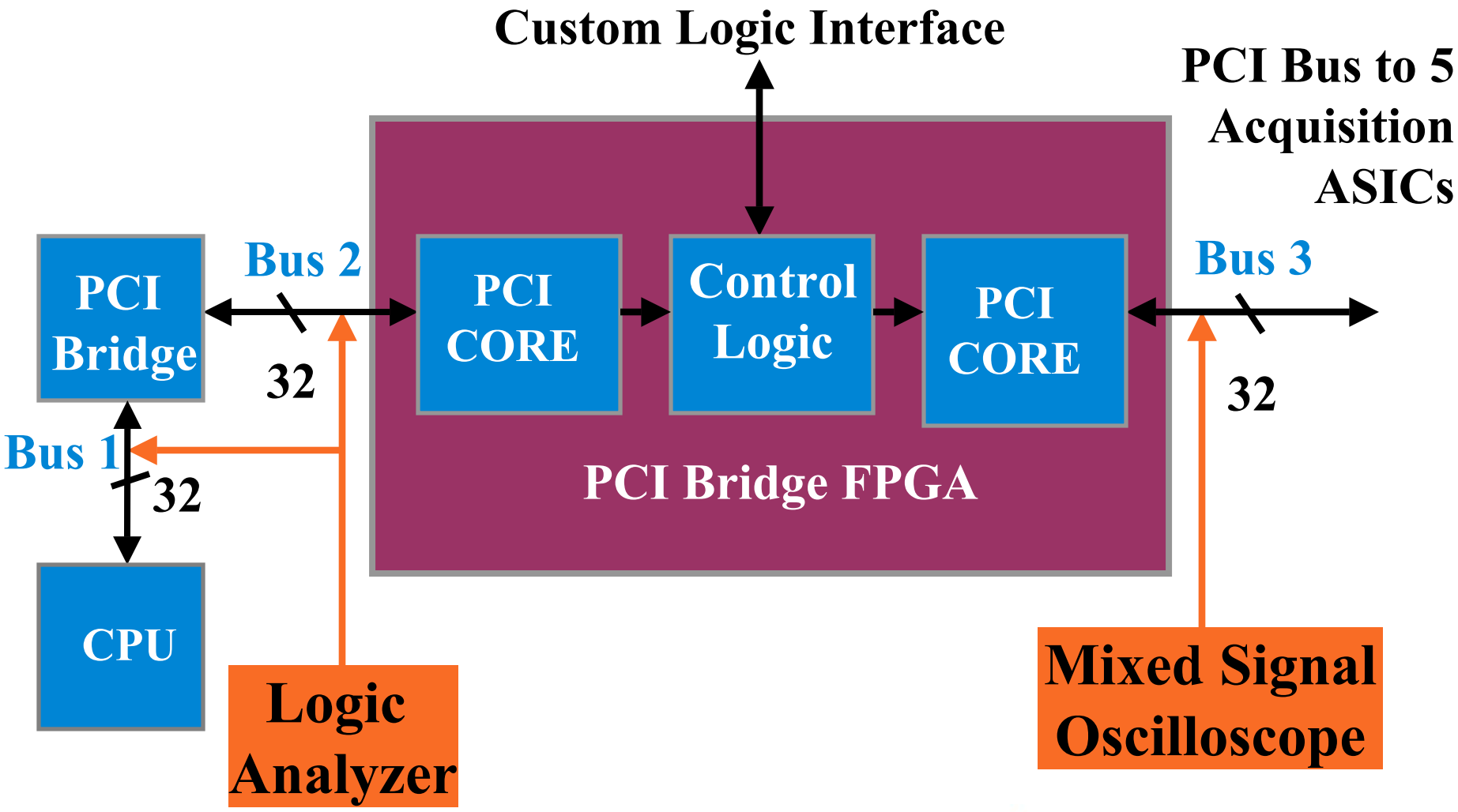
Agilent Technologies

Hint #24: Functional or Parametric?

Functional	Either	Parametric
Duplicates in Simulation	Caused by Temperature	Observed with Scope
Observed with Logic Analyzer or Debugger	Varies with Code or HDL	
	Follows Board or Chip	

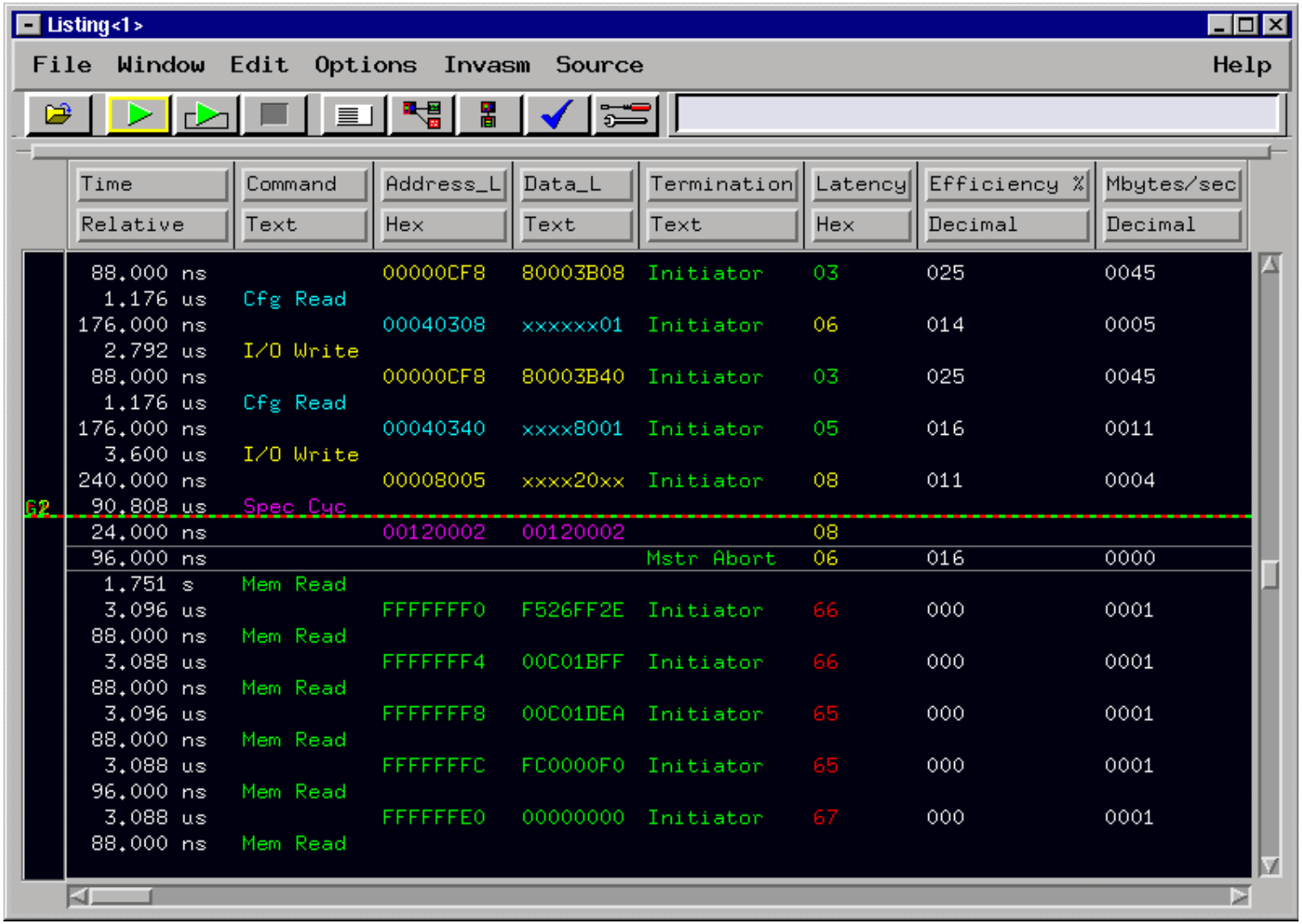
Agilent Technologies

Debug Environment



Agilent Technologies

Logic Analyzer Isolates Fault



Time	Command	Address_L	Data_L	Termination	Latency	Efficiency %	Mbytes/sec
Relative	Text	Hex	Text	Text	Hex	Decimal	Decimal
88.000 ns		00000CF8	80003B08	Initiator	03	025	0045
1.176 us	Cfg Read						
176.000 ns		00040308	xxxxxx01	Initiator	06	014	0005
2.792 us	I/O Write						
88.000 ns		00000CF8	80003B40	Initiator	03	025	0045
1.176 us	Cfg Read						
176.000 ns		00040340	xxxx8001	Initiator	05	016	0011
3.600 us	I/O Write						
240.000 ns		00008005	xxxx20xx	Initiator	08	011	0004
GP 90.808 us	Spec Cyc						
24.000 ns		00120002	00120002		08		
96.000 ns				Mstr Abort	06	016	0000
1.751 s	Mem Read						
3.096 us		FFFFFFF0	F526FF2E	Initiator	66	000	0001
88.000 ns	Mem Read						
3.088 us		FFFFFFF4	00C01BFF	Initiator	66	000	0001
88.000 ns	Mem Read						
3.096 us		FFFFFFF8	00C01DEA	Initiator	65	000	0001
88.000 ns	Mem Read						
3.088 us		FFFFFFFC	FC0000F0	Initiator	65	000	0001
96.000 ns	Mem Read						
3.088 us		FFFFFFE0	00000000	Initiator	67	000	0001
88.000 ns	Mem Read						

Agilent Technologies

MSO Finds Root Cause

Analog channels see isolated clock coupling

Digital channels provide state trigger on first address phase after a bus turnaround

Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- “Late in the Game” Debug Process Recommendations
- Recommended Agilent Products
- Additional References

Agilent Technologies

34401A 6 1/2 Digit DMM

- $1,163
- Accurate
- Fast
- Easy to Read
- Reliable

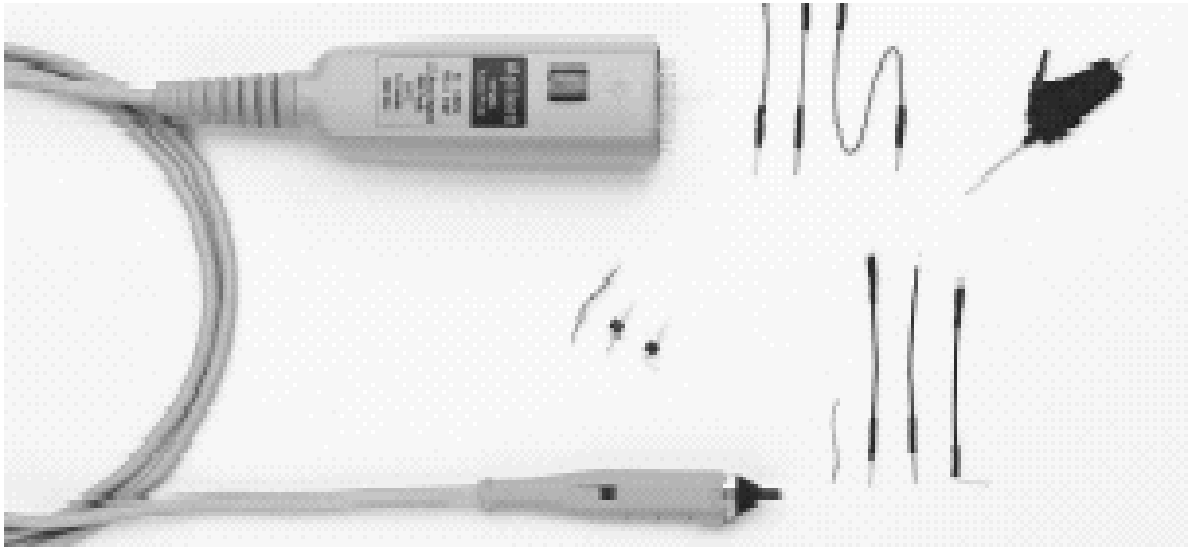
For more information on the 33401 Digital Multimeter, and other low-cost benchtop instruments,

visit www.agilent.com/find/everydaytools

Agilent Technologies

1156A 1.5GHz Active Probe

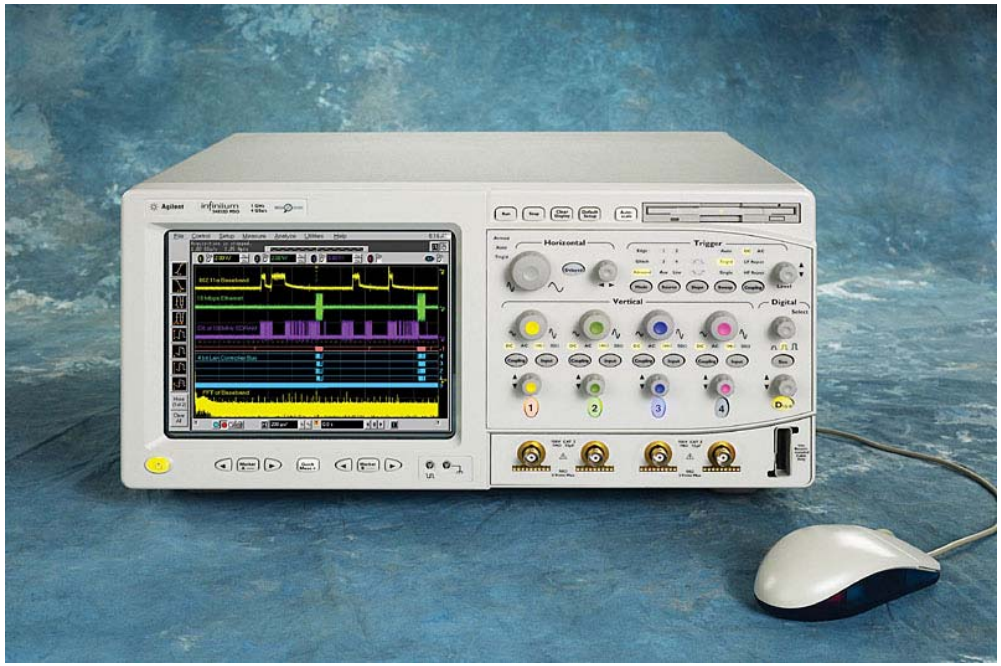
- $1,866
- Damped Accessories for Minimized Loading
- Small Size
- Documented BW for Recommended Accessories



Agilent Technologies

Agilent Infiniium MSOs

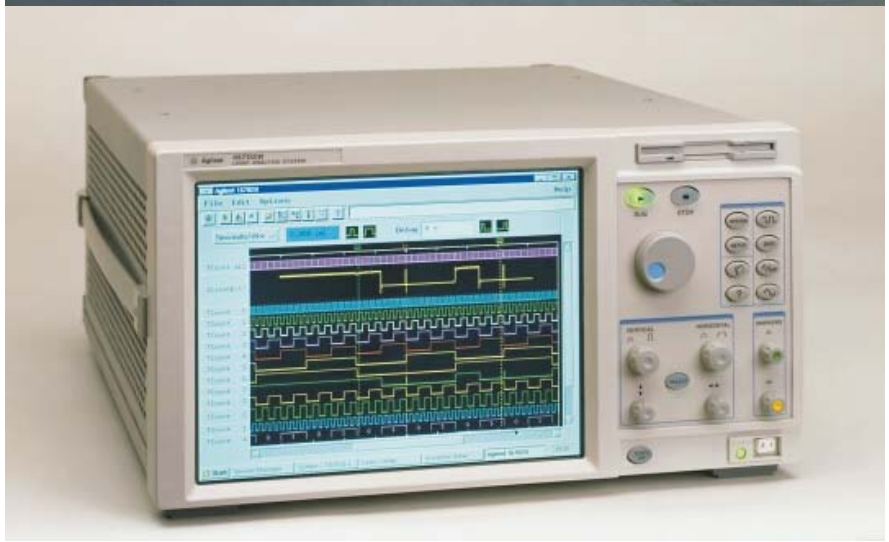
- $17K - $25K
- 600MHz and 1GHz
- 2+16 and 4+16 channel models
- MegaZoom Deep Memory
- 2M/channel Standard
- 8M/channel Optional
- http://www.agilent.com/find/mso



Agilent Technologies

Agilent Logic Analyzer Family

- Modular, Standalone and PC Hosted models
- Wide variety of speed and channel count configurations
- Wide variety of probing solutions
- http://www.agilent.com/find/logic



Agilent Technologies

E5850A Time Correlation Fixture

- Automatic Deskew
- Combined Display
- Tracking Markers

Agilent Technologies

Agenda

- Trends in Embedded Systems
- SDRAM and PCI Overview
- Turn on Process Recommendations
- “Late in the Game” Debug Process Recommendations
- Recommended Agilent Products
- Additional References

Agilent Technologies

Recommended App Notes

- Debugging a PCI Bus with a Mixed-Signal Oscilloscope - Pub # 5988-7745EN
- Customer Validates Signal Integrity on 100 MHz DDR SDRAM With Mixed-Signal Oscilloscope - Pub # 5988-9265EN
- The Truth About the Fidelity of High-Bandwidth Voltage Probes - Pub # 5988-6515EN
- http://www.measurement.tm.agilent.com/new/category704.html

Agilent Technologies

Recommended Books

- Johnson, Howard W., *High Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993
- Witte, Robert A., *Electronic Test Instruments,* Prentice Hall, 1993
- Ganssle, Jack, *The Art of Designing Embedded Systems*, Newnes, 2000

Thank You For Attending

Debug Your Embedded System More Quickly

Agilent Technologies